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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,026	07/17/2003	Whay Sing Lee	SUNMP232	4465

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EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 10/623,026	Applicant(s) LEE ET AL.	
	Examiner Tuan V. Thai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-28* is/are pending in the application.

4a) Of the above claim(s) *19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,12,20-22 and 24-26* is/are rejected.

7)☒ Claim(s) *6,10,11,13-18,23,27 and 28* is/are objected to.

8)☒ Claim(s) *19* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed January 17, 2006. Applicant's election without traverse of group I, claims 1-18 and 20-28 in the reply filed on January 17, 2006 is acknowledged. Claim 19 has been canceled due to non-elected group of claim. Claims 1-18 and 20-28 are presented for examination

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the

English language.

4. Claims 1-3, 12, 20-22 and 24-26 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sindhu et al.; (USPN: 6,493,347); hereinafter Sindhu.

As per claim 1; Sindhu teaches the invention as claimed including a switch 100 (e.g. see figure 2B) comprises a set of inputs (150-0 to 150-3, e.g. see figure 2B); a set of memory banks (150-0 to 150-3) being equal in number to the set of inputs (e.g. see figure 2B), each input capable of transferring a data stream into the set of memory banks (e.g. see column 5, lines 57 et seq.), wherein the data stream of each input is to be distributed across each of the set of memory banks (e.g. see abstract, column 2, lines 30 et seq., and lines 42 et seq.); and a set of outputs 150-0 to 150-3 (e.g. see figure 2B), the set of outputs being equal in number to the set of memory banks (e.g. see figure 2B), each data stream that is distributed across each of the set of memory banks is to be output from at least one of the set of outputs (e.g. see abstract; column 2, lines 32 et seq.).

As per claim 2, wherein the data stream of each input is to be distributed across each of the set of memory banks such that each of the set of memory banks receives one or more differing portions of the data stream (e.g. see column 2, lines 30 et seq.;

column 3, lines 19 et seq., abstract);

As per claim 3, the further limitation of wherein the data stream that is distributed across each of the set of memory banks is to be output from at least one of the set of outputs by retrieving the one or more differing portions of the data stream and transmitting the one or more differing portions of the data stream to the at least one of the set of outputs in a sequence that provides the data stream is taught by Sindhu, for example Sindhu discloses that Linking information is stored in one bank of the memory for linking cells of the data packet that are stored throughout the distributed memory. The linking information is used for extracting the cells in order for transmission from the router to the destination. (e.g. see column 3, lines 24 et seq.);

As per claim 12, Sindhu discloses a memory 104 comprises a number of inputs, each input capable of receiving a data stream to be stored in the memory (e.g. see figure 2B); a number of memory banks 150-1 to 150-3 for storing data streams received by the number of inputs (e.g. see figure 2B), the number of memory banks being equal to the number of inputs (e.g. see figure 2B); a first ratcheting distributor 100 for distributing the data stream received by either of the number of inputs across the number of memory banks whereby one or more of the number of memory banks contains a distinct portion of the data stream (e.g. see figure

2B; column 12, lines 32 et seq. and abstract); a number of outputs 150-0 to 150-3, each output capable of providing the data stream previously stored in the memory (e.g. see figure 2B); and a second ratcheting distributor 102 (e.g. see figure 2B) for providing the distinct portion of the data stream contained within either of the number of memory banks to either of the number of outputs (e.g. see column 8, lines 44 et seq.; column 11, lines 11 et seq.);

As per claim 20; it encompasses the same scope of invention as to that of claim 1 except that it is drafted as method format rather apparatus format, the claim is therefore rejected for the same reasons as being set forth above, the further limitation of each of the number of inputs being received simultaneously is taught by Sindhu, for example, each port could simultaneously be outputting packets as well as receiving new data packets (e.g. see column 2, lines 4 et seq.);

As per claim 21, Sindhu discloses using a ratcheting distributor as being equivalent to switch 100 to distribute the data stream associated with each of the number of inputs across the number of memory banks (e.g. see figure 2B);

As per claim 22, Sindhu clearly teaches Round robin data handler 500 time division *multiplexes the transfers to output processor 505 such that consecutive cells from the same multi-function multiport are written to consecutive memory banks 105*

(modulo N) in global data buffer 104 (e.g. see column 8, lines 44 et seq.);

As per claim 24, Sindhu discloses retrieving the portion of the data stream stored in each of the number of memory banks; and transmitting the portion of the data stream stored in each of the number of memory banks to an output, the transmitting causing the data stream to be provided at the output (e.g. see column 11, lines 11 et seq., column 20, lines 44 et seq.);

As per claim 25, wherein the retrieving and the transmitting of the portion of the data stream stored in each of the number of memory banks is perform simultaneously for a number of data streams, each of the number of data streams being transmitted to different outputs (e.g. see abstract, column 2, lines 4 et seq.);

As per claim 26, using a ratcheting distributor 100 and 102 to retrieve and transmit the portion of the data stream stored in each of the number of memory banks (e.g. see figure 2B and abstract);

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

> the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-5, 7 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sindhu (USPN: 6,493,347);

As per claims 4 and 7; Sindhu discloses the invention substantially as claimed, detailed above with respect to claims 1-3. Sindhu however does not particularly teach a first set of multiplexers being used where, each of the first set of multiplexers connected to receive the set of inputs, each of the first set of multiplexers having a multiplexer output connected to one of the set of memory banks, each of the set of memory banks being connected to one of the first set of multiplexers, each of the first set of multiplexers connected to receive a selector signal for controlling which of the received set of inputs is to be transmitted to the multiplexer output in a given clock cycle. First of all, it should be noted that Sindhu clearly teaches Round robin data handler 500 time division ***<u>multiplexes</u> the transfers to output processor 505 such that consecutive cells from the same multi-function multiport are written to consecutive memory banks 105 (modulo N) in global data buffer 104*** (e.g. see column 8, lines 44 et seq.); secondly multiplexer devices are well known in the art for performing such functions. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current

invention was made to implement the first set of multiplexer circuits within the Round Robin data handler 500 of Sindhu for controlling which of the received set of inputs is to be transmitted to the multiplexer output in a given clock cycle to route data to one of the set of memory banks. In using a first set of multiplexer, it would cause a selective data to be properly routed to different memory banks, minimizing data overlapping and data-transfer-error rate, therefore being advantageous.

As per claim 5, Sindhu discloses a sequence of single bit signals being equal in number to the set of inputs as being equivalent to input switch 100 receives a total of N cells which is equal to the number of multi-function multiports (e.g. see column 7, lines 36 et seq.);

As per claim 8, as detailed above with respect to claims 4 and 7; Sindhu clearly teaches Round robin data handler 500 time division ***multiplexes*** ***the transfers to output processor 505 such that consecutive cells from the same multi-function multiport are written to consecutive memory banks 105 (modulo N) in global data buffer 104*** (e.g. see column 8, lines 44 et seq.); secondly multiplexer devices are well known in the art for performing such functions. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the second set of multiplexer

circuits within the Round Robin data handler 500 of switch 102 for controlling which of the received multiplexer input from each of the set of the memory banks is to be transmitted to the multiplexer output in a given clock cycle. First, in using a second set of multiplexer, it would cause a selective data to be properly routed to different output section, minimizing data overlapping and data-transfer-error rate; secondly, an advantage in having a separate second multiplexer set is that the bit rate determination procedure can be achieved by carefully re-organizing the data, therefore being advantageous.

As per claim 9, Sindhu discloses input switch 100 receives a total of N cells which is equal to the number of multi-function multiports (e.g. see column 7, lines 36 et seq.);

Allowable subject matter

7. Claims 6, 10, 11, 13, 16, 23 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The prior arts of record do not teach nor disclose ... Claims 14-15, 17-18 and 28 are also allowable since they are depended upon the indicated allowable claims 13, 16 and 27.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/January 31, 2006

Tuan V. Thai

PRIMARY EXAMINER

Group 2100